

AMD Athlon™ 64

Product Data Sheet



- **Compatible with Existing 32-Bit Code Base**
 - Including support for SSE, SSE2, MMX™, 3DNow!™ technology and legacy x86 instructions
 - Runs existing operating systems and drivers
 - Local APIC on-chip
- **AMD64 Technology**
 - AMD64 technology instruction set extensions
 - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
 - Eight new 64-bit integer registers (16 total)
 - Eight new 128-bit SSE/SSE2 registers (16 total)
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
 - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
 - With advanced branch prediction
- **16-Way Associative ECC-Protected L2 Cache**
 - Exclusive cache architecture—storage in addition to L1 caches
 - 1 Mbyte, 512-Kbyte and 256-Kbyte options
- **Machine Check Architecture**
 - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
 - Multiple low-power states
 - System Management Mode (SMM)
 - ACPI compliant, including support for processor performance states
- **Electrical Interfaces**
 - HyperTransport™ Technology: LVDS-like differential, unidirectional
 - DDR SDRAM: SSTL_2 per JEDEC specification
 - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications

754 Pin Package Specific Features

- **Refer to the *AMD Functional Data Sheet, 754 Pin Package, order# 31410*, for functional, electrical, and mechanical details of 754 pin package processors**
- **Packaging**
 - 754 pin lidded micro PGA
 - 1.27-mm pin pitch
 - 29x29 row pin array
 - 40mm x 40mm organic substrate
 - Organic C4 die attach
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 64-bit DDR SDRAM at 100, 133, 166, and 200 MHz
 - Supports up to three unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gigabytes/s in each direction

939 Pin Package Specific Features

- **Refer to the *AMD Functional Data Sheet, 939 Pin Package, order# 31411*, for functional, electrical, and mechanical details of 939 pin package processors**
- **Packaging**
 - 939 pin lidded micro PGA
 - 1.27-mm pin pitch
 - 31x31 row pin array
 - 40mm x 40mm organic substrate
 - Organic C4 die attach
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 128-bit DDR SDRAM at 100, 133, 166, and 200 MHz
 - Supports up to four unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

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